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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,903	02/27/2002	Carl Mizuyabu	1376.0200100	4958

34456 7590 01/06/2005

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,903	MIZUYABU ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 43 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 - 8, 13, 19 – 20, and 36 – 37, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1.

4. As to claims 1, and 36, Mirov discloses an apparatus and method comprising:

a. determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40];

b. disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and

c. providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 – 67, col. 5, lines 1 – 8, col. 6, lines 49 – 67, col. 7, lines 1 – 20, col. 8, lines 65 – 67, col. 9, lines 1 – 14, col. 13, lines 14 – 52, col. 15, lines 64- 67, col. 16, lines 1 – 67, col. 17, lines 1 – 54, fig. 5].

5. As to claims 2 – 3, Mirov teaches that the device [apparatus] with different operating modes with reduced power consumption [col.4, lines 46 – 67].

6. As to claims 4 – 5, Mirov discloses clock generator, a phase locked loop circuit, and a bypass circuit for a computer system with an input clock signal [CLK IN] therefore he teaches different ways of generating clock using crystal oscillator, through RC circuit too.

7. As to claims 6, and 7, Mirov discloses coupling of an output of the phase locked loop to a clock divider [1006][col. 12, lines 54 – 57, fig. 5].

8. As to claim 8, Mirov teaches a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device [col. 21, lines 27 – 67, col. 22, lines 1 – 67, col. 23, lines 1 – 56,fig. 18].

9. As to claim 13, Mirov discloses device including portable electronic device [laptop computers][col. 1, line16 – 17].

10. As to claim 19, Mirov discloses enabling/disabling the power modules to produce desired voltage and make available the desired current on a line for different operating modes [col. 21, lines 47 – 67, col. 22, lines 36 – 67].

11. As to claim 20, Mirov discloses providing the oscillator signal [CLOCK IN] to drive a clock line includes coupling [1012, clock tree] a line carrying the oscillator signal [CLOCK IN] to the clock line [CLOCK OUT][col. 16, lines 16 – 18, fig. 10].

12. As to claims 35, and 37, Mirov teaches that the device [apparatus] with different operating modes with reduced power consumption [col.4, lines 46 – 67].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 as applied to claims 1, and 13 as above.

15. As to claim 14, Mirov discloses an apparatus and method for reducing power consumption of an electronic device such as laptop computers [portable] drawing power from battery [battery operated] [col. 1, lines 17 – 20] but does not specify what type of electronic devices. The examiner takes Official Notice that laptop and personal digital assistant device [PDA] are well-known types of battery operated portable devices. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention to use a laptop computers or personal digital assistant device for the portable electronic device disclosed by Mirov.

16. Claims 1 – 13, 15 - 20, 24, 26 – 28, 35, and 36 – 37, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1, and further in view of Mann et al. [hereinafter as Mann], US Patent 5,877,656.

17. As to claims 1, 24, and 36, Mirov discloses an apparatus and method for reducing power consumption comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop

to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 – 67, col. 5, lines 1 – 8, col. 6, lines 49 – 67, col. 7, lines 1 – 20, col. 8, lines 65 – 67, col. 9, lines 1 – 14, col. 13, lines 14 – 52, col. 15, lines 64- 67, col. 16, lines 1 – 67, col. 17, lines 1 – 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer [162], and system clock PLL [144] with PLL output through [154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 – 67, col. 5, lines 1 – 63, fig. 2].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Mann before him at the time of invention was made, to modify the circuit arrangement for receiving input clock signal and driving output signals disclosed by Mirov to include a clock generation with crystal oscillator with use of input/output buffer for driving signals to/from logical blocks, and multiplexer for selectively selecting input signal and driving to an output as taught by Mann in order to obtain PLL-based clock generator which can be electrically configured, erased prior to packaging, reduces cycle time from customer requests to prototypes,

and reduces inventory costs and can be field programmed if desired [col. 2, lines 1 – 16, col. 6, lines 60 – 67].

18. As to claims 2 – 3, Mirov teaches that the device [apparatus] with different operating modes with reduced power consumption [col.4, lines 46 – 67].

19. As to claims 4 – 5, Mirov discloses clock generator, a phase locked loop circuit, and a bypass circuit for a computer system with an input clock signal [CLK IN] therefore he teaches different ways of generating clock using crystal oscillator, through RC circuit too.

20. As to claims 6, and 7, Mirov discloses coupling of an output of the phase locked loop to a clock divider [1006][col. 12, lines 54 – 57, fig. 5].

21. As to claim 8, Mirov teaches a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device [col. 21, lines 27 – 67, col. 22, lines 1 – 67, col. 23, lines 1 – 56,fig. 18].

22. As to claim 13, Mirov discloses device including portable electronic device [laptop computers][col. 1, line16 – 17].

23. As to claim 19, Mirov discloses enabling/disabling the power modules to produce desired voltage and make available the desired current on a line for different operating modes [col. 21, lines 47 – 67, col. 22, lines 36 – 67].

24. As to claim 20, Mirov discloses providing the oscillator signal [CLOCK IN] to drive a clock line includes coupling [1012, clock tree] a line carrying the oscillator signal [CLOCK IN] to the clock line [CLOCK OUT][col. 16, lines 16 – 18, fig. 10].

25. As to claim 26, Mirov discloses a first clock divider [1006] coupled between the first multiplexor [1010] and the first clock line [CLOCK IN], said first clock divider [1006] to

provide a divided clock signal to the second clock line [CLK OUT], wherein the divided clock signal is based on the locked clock signal, when in the first power mode, and based on the source clock signal, when in the second power mode [col. 12, lines 48 – 65, col. 16, lines 9 – 67, col. 17, lines 1 – 16, fig. 10].

26. As to claim 27, Mann discloses a frequency generator [10] with different oscillator to generate source clock signal [152], therefore he teaches a very well known resistor/capacitor circuit to generate source clock signal too [fig. 2].

27. As to claim 28, Mann discloses a frequency generator [10] with oscillator, which includes a crystal oscillator [142] to generate said source clock signal [152][fig. 2].

28. As to claims 35, and 37, Mirov teaches that the device [apparatus] with different operating modes with reduced power consumption [col.4, lines 46 – 67].

29. Claims 9 – 12, 16 – 18, 25, 28, and 39 – 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1, and further in view of Mann et al. [hereinafter as Mann], US Patent 5,877,656 as applied to claims 1, 24, and 36, above, and further in view of Zhang et al. [hereinafter as Zhang], US Patent 6,687,322.

30. As to claim 25, Mirov discloses an apparatus and method for reducing power consumption comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 –

67, col. 5, lines 1 – 8, col. 6, lines 49 – 67, col. 7, lines 1 – 20, col. 8, lines 65 – 67, col. 9, lines 1 – 14, col. 13, lines 14 – 52, col. 15, lines 64- 67, col. 16, lines 1 – 67, col. 17, lines 1 – 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer [162], and system clock PLL [144] with PLL output through [154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 – 67, col. 5, lines 1 – 63, fig. 2].

However, neither Mirov nor Mann teaches a second multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to: when in a first power mode, pass said source clock signal to said third input/output buffer; and when in a second power mode, pass said locked clock signal to said third input/output buffer; a second clock line coupled to the third input/output buffer of the second multiplexor.

Zhang discloses dual mode clock alignment and distribution with a second multiplexor [510] having a first input/output buffer coupled to the input/output buffer [502] of the oscillator,

a second input/output buffer coupled to the second input output buffer of the phase locked loop [PLLOUT] and a third input/output buffer, said multiplexor to: when in a first power mode [low speed], pass said source clock signal to said third input/output buffer [514]; and when in a second power mode [high speed], pass said locked clock signal to said third input/output buffer; a second clock line [CLKO] coupled to the third input/output buffer [514] of the second multiplexor [510] [col. 5, lines 9 – 67, col. 6, lines 1 – 60, fig. 5].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov, Mann, and Zhang before him at the time of invention was made, to modify the circuit arrangement for receiving input clock signal to include a clock generation with crystal oscillator with use of input/output buffer for driving signals to/from logical blocks, and multiplexer for selectively selecting input signal and driving to an output and driving output signals disclosed by Mirov and Mann to include a second multiplexor as taught by Zhang in order to obtain dual mode clock alignment and distribution devices bypasses the PLL and generates clock with sufficient margins to accommodate the requirements of the PCI mode and support both both lower speed PCI clocking mode and the higher speed PCI-X clocking mode to provide substantial savings in cost while reducing circuit complexity [co. 3, lines 34 – 51].

31. As to claims 9, and 15, Zhang discloses the step of disabling the phase lock loop, when in first power mode [lower speed or PCI clock mode] which inherently teaches [as per PCI-X specs] including reducing in comparison to a maximum number of bits used available [PCI-X mode] used to represent multimedia data [col. lines 4 – 21].

32. As to claims 10 – 11, 16 – 17, and 39 – 40, Zhang discloses PCI and PCI-X devices therefore he teaches multimedia data including audio, video data [col. 2, lines56 – 57, col. lines 4 – 21].

33. As to claims 12, and 18, Zhang discloses providing the oscillator signal [CLKin from 502] to the phase locked loop [504], when in the second power mode [high speed or PCI-X], which includes use of maximum number of bits to represent multimedia data [col. 3, lines 33 – 51, fig. 5].

34. As to claim 28, Mann discloses a frequency generator [10] with oscillator which includes a crystal oscillator [142] to generate said source clock signal [152][fig. 2].

35. Claims 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1, and further in view of Mann et al. [hereinafter as Mann], US Patent 5,877,656, further in view of Zhang et al. [hereinafter as Zhang], US Patent 6,687,322 as applied to claims 24 - 25, above, and further in view of Durham et al. [hereinafter as Durham], US Patent 6,785,829 B1.

36. As to claims 29 – 33, neither Mirov nor Mann, nor Zhang does teach steps of identifying a number of pending instructions and types of pending instructions for determining the power mode for a device. In summary, he does not teach to determine the time to enter low power mode based on types, and number of pending instructions to be performed.

Durham teaches method and apparatus with low power mode identifying circuit [determining low power mode] including power audit and control circuit for monitoring power dissipation of functional unit within processor. The low power mode circuit [234] examines the low power mode enable signal, the request signal and determine the best time to enter the low

power mode depending upon types and number of pending operations or instructions to be performed by the functional unit [col. 6, lines 41 – 67, col. 7, lines 1 – 16, col. 2, lines 4 – 35, col. 3, lines 26 – 67, col. 4, lines 1 - 24].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Durham before him at the time of invention was made, to modify the method and apparatus for reducing power consumption disclosed by Mirov to include a power audit and control circuit for power monitoring including steps of determining types and number of pending instructions to be performed and determine the best time to enter the low power mode as taught by Durham in order to obtain self audit and control of power within functional unit of processor for selectively entering low power mode on per functional unit basis to reduce power dissipation of functional unit [col. 1, lines 57 – 64] and each unit can implement its own power dissipation savings easier and more efficiently than central power dissipation control unit [col. 3, lines 44 – 62].

37. Claims 21 – 22, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1 as applied to claims 1, 24, and 36 above, and further in view of Durham et al. [hereinafter as Durham], US Patent 6,785,829 B1.

38. As to claims 21 - 22, 41, and 43, Mirov discloses an apparatus and method comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 – 67, col. 5, lines 1

– 8, col. 6, lines 49 – 67, col. 7, lines 1 – 20, col. 8, lines 65 – 67, col. 9, lines 1 – 14, col. 13, lines 14 – 52, col. 15, lines 64- 67, col. 16, lines 1 – 67, col. 17, lines 1 – 54, fig. 5].

However, Mirov does not teach steps of identifying a number of pending instructions and types of pending instructions for determining the power mode for a device. In summary, he does not teach to determine the time to enter low power mode based on types, and number of pending instructions to be performed.

Durham teaches method and apparatus with low power mode identifying circuit [determining low power mode] including power audit and control circuit for monitoring power dissipation of functional unit within processor. The low power mode circuit [234] examines the low power mode enable signal, the request signal and determine the best time to enter the low power mode depending upon types and number of pending operations or instructions to be performed by the functional unit [col. 6, lines 41 – 67, col. 7, lines 1 – 16, col. 2, lines 4 – 35, col. 3, lines 26 – 67, col. 4, lines 1 - 24].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Durham before him at the time of invention was made, to modify the method and apparatus for reducing power consumption disclosed by Mirov to include a power audit and control circuit for power monitoring including steps of determining types and number of pending instructions to be performed and determine the best time to enter the low power mode as taught by Durham in order to obtain self audit and control of power within functional unit of processor for selectively entering low power mode on per functional unit basis to reduce power dissipation of functional unit [col. 1, lines 57 – 64] and each unit can implement its own power dissipation savings easier and more efficiently than central power dissipation control unit [col. 3, lines 44 – 62].

39. Claims 23, 34, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirov et al. [hereinafter as Mirov], US Patent 6,691,215 B1, and further in view of Mann et al. [hereinafter as Mann]; US Patent 5,877,656 as applied to claims 1, 24, and 36 above, and further in view of Anwyl et al. [hereinafter as Anwyl], US Patent 5,576,738.

40. As to claims 23, 34, and 42, Mirov discloses an apparatus and method for reducing power consumption comprising: determining [based on the bits] a power mode [power mode] for a device [col. 17, 28 – 40]; disabling a phase locked loop [by asserting PLL BYPASS signal] and providing an oscillator signal [CLOCK IN] to drive a clock line [CLOCK OUT] when in a first power mode [idle mode]; and providing the oscillator signal [CLOCK IN] to an input of the phase locked loop [PLL] and providing a locked signal from an output of the phase locked loop to the dock line [CLOCK OUT] when in a second power mode [active mode][col. 4, lines 43 – 67, col. 5, lines 1 – 8, col. 6, lines 49 – 67, col. 7, lines 1 – 20, col. 8, lines 65 – 67, col. 9, lines 1 – 14, col. 13, lines 14 – 52, col. 15, lines 64- 67, col. 16, lines 1 – 67, col. 17, lines 1 – 54, fig. 5].

However, Mirov does not teach arrangement of clock input in detail with commonly used oscillator for clock signal generation and input/output buffer to provide signal as input to and to drive an output signal from different logical circuit blocks. In summary, Mirov does not teach the use of oscillator and input/output buffer in clock generation and selectively driving the output signal.

Mann discloses an architecture for a programmable clock generator [100, fig. 2] having an input section, clock section, and output section with reference crystal oscillator [142] receives input from reference crystal of input section [101] and output a reference signal through an output line [152] to reference buffer [162], and system clock PLL [144] with PLL output through

[154] via multiplexer for selectively driving selected input to output section buffer [104] [col. 4, lines 45 – 67, col. 5, lines 1 – 63, fig. 2].

However, neither Mirov nor Mann, does teach step determining the power mode includes identifying a change in display content. In summary, they do not teach to determine to activate/deactivate the power mode to and from standby mode based on change in display content.

Anwyl teaches system with display apparatus with means for detecting changes in image content between successive frames of input video and method of determining the power mode of display device [by bringing out of low power "standby mode" in response to change in screen content to displayed][col. 4, lines 44 – 67, col. 5, lines 1 – 16].

It would have been obvious to one of ordinary skill in art, having the teachings of Mirov and Mann before him at the time of invention was made, to modify the system for reduced power consumption disclosed by Mirov and Mann to include activation/deactivation of low power mode based on identifying a change in display content [change in screen content between successive frame input video signals] as disclosed by Anwyl in order to obtain a display with power management for controlling display circuitry [col. 4, lines 44 – 67, col. 5, lines 1 – 16].

41. **Examiner's note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references

in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

42. Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
December 27, 2004